

100G CFP2 to QSFP28 Adapter

SL-CFP2-QSFP28



Overview

The 100G CFP2 to QSFP28 Adapter module is a four-Channel, high performance, hot pluggable, and interconnect solution supporting 100G Ethernet and Telecom. The adapter converts a CFP MSA interface to 1-port of 100GE QSFP28. It is compliant with the CFP MSA. Sourcelight 100G CFP2 to QSFP28 Adapter integrates four data lanes in each direction with operating at up to 28Gbps per lane. The adapter is without the FEC (Forward Error Correction) and supports 100G QSFP28 LR4/ER4. When the 100GE network equipment’s CFP2 port has FEC function, it can support 100G QSFP28 SR4/PSM4/CWDM4/CLR4.

Features

- ◆ Compliant to CFP2 Hardware Specification Version 1.0
- ◆ Compliant to CFP2 MSA Management Interface Specification Version 2.4
- ◆ 4 channels full-duplex transceiver
- ◆ Internal CDR circuits on both receiver and transmitter channels
- ◆ Transmission data rate up to 28Gbps per channel
- ◆ OTU4 compatible
- ◆ Without FEC (Forward Error Correction)
- ◆ 1 port QSFP28 TX&RX, supports 100G QSFP28 LR4/ER4.
- ◆ Supports 100G QSFP28 SR4/PSM4/CWDM4/CLR4 (when the 100GE network equipment’s CFP2 port has FEC function)
- ◆ MDIO digital diagnostic interface and control capabilities
- ◆ Power class 3 (Adapter<2W max)
- ◆ Hot pluggable electrical interface
- ◆ Operating case temperature:0°C~ +70°C
- ◆ Single 3.3V power supply
- ◆ RoHS 6 compliant (lead free)

Applications

- ◆ 100GBE interconnects, IEEE 802.3ba 100GBASE-LR4(Adapter+QSFP28_LR4)
- ◆ High-speed core router connections& Datacom/Telecom switch
- ◆ Data aggregation and backplane applications
- ◆ Proprietary protocol and density application

Ordering Information

Part Number	Product Description
SL-CFP2-QSFP28	100G CFP2 to QSFP28 Adapter, without FEC

Adapter Block Diagram

As showed in Figure 1, the adapter converts 4 parallel electrical data inputs to 4 parallel electrical data output signals through CDR circuits on both receiver and transmitter side.

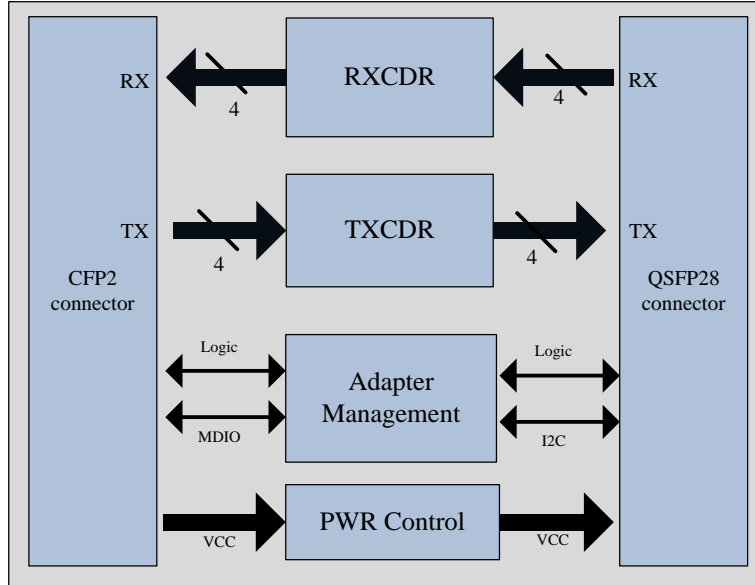


Figure1. Adapter Block Diagram

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	Vcc	-0.5	3.6	V
Input Voltage	Vin	-0.3	Vcc+0.3	V
Storage Temperature	Tst	-20	85	°C
Humidity(non-condensing)	Rh	5	85	%

*Exceeding any one of these values may destroy the device immediately

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Supply Voltage	Vcc	3.13	3.3	3.47	V
Operating Case temperature	Tca	0		70	°C
Data Rate Per Lane	fd	-	25.78125	27.952	Gbps
Power Dissipation	Pm			2	W
Low Power Mode Dissipation	Plow			2	W
Aggregate Bit Rate	BRaggr		103.125	111.8	Gbps

Electrical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Notes	
Differential input impedance	Zin	90	100	110	ohm		
Differential Output impedance	Zout	90	100	110	ohm		
25GBE	Differential input voltage amplitude	ΔVin	300		900	mVp-p	1
	Differential output voltage amplitude	ΔVout	400		800	mVp-p	2
Bit Error Rate	BER			E-12		3	
Input Logic Level High	VIH	2.0		VCC+0.3	V	3.3V LVCOMS	
		0.84		1.5	V	1.2V LVCOMS	
Input Logic Level Low	VIL	-0.3		0.8	V	3.3V LVCOMS	
		-0.3		0.36	V	1.2V LVCOMS	
Output Logic Level High	VOH	VCC-0.2		VCC	V	3.3V LVCOMS	
		1.0		1.5	V	1.2V LVCOMS	
Output Logic Level Low	VOL	0		0.2	V	3.3V LVCOMS	
		-0.3		0.2	V	1.2V LVCOMS	

Note:

1. Differential input voltage amplitude is measured between TxnP and TxnN.
2. Differential output voltage amplitude is measured between RxnP and RxnN.
3. BER=10⁻¹²; PRBS 2³¹-1@25.78125Gbps.

Register Map

100G CFP2 to QSFP28 Adapter is compliant to CFP MSA Management Interface Specification Version 2.4. The addresses correspond to CFP MSA Management Interface Specification V2p4rev06b. Not all the QSFP28 I2C registers are remapped. Some registers are illustrated in Table 1. Other registers also correspond to CFP MSA MDIO MIS(Management Interface Specification V2p4rev06b). The QSFP28 I2C registers(DDM Monitor and Alarm/Warning register) are remapped into the CFP MDIO register map. The Adapter can provide CFP Module State transition, FAWS signal, User NVR Restore and Save Functions and DDM monitor. It makes the optic look exactly like a CFP2 module.

Some of the 100G CFP2 to QSFP28 Adapter register

CFP NVR 1 Table. Basic ID registers.			
HexAddr	Register Name	Description	Note
8000	Module Identifier	Default value is 11h: CFP2	1
8001	Extended Identifier	Default value is A0h: Power Class 3, Parallel type	1
8002	Connector Type Code	The value corresponds to QSFP28 I2C register(Address A0h, byte 130(Page 00))	1,2
8003	Ethernet Application Code	Default value is 01h: 100GE-LR4	1
8004~8007	Application Code	Default value is 00h:Undefined type	1

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8008	Additional Capable Rates Supported	Default value is 18h:Support 111.8 Gbps and 103.125 Gbps	1
8009	Number of Lanes Supported	Default value is 44h: 4 Network Lanes and 4 Host Lanes	1
800A	Media Properties	Default value is 84h	1
800B	Maximum Network Lane Bit Rate	Default value is 8Ch: 28Gbps	1
800C	Maximum Host Lane Bit Rate	Default value is 8Ch: 28Gbps	1
800D	Maximum Single Mode Optical Fiber Length	Default value is 0Ah: 10km	1
800E	Maximum Multi-Mode Optical Fiber Length	Default value is 1Eh: 300m	1
800F	Maximum Copper Cable Length	Default value is 00h: undefined	1
8010	Number of Active Transmit Fibers	Default value is 00h: undefined	1
8011	Number of Wavelengths per active Transmit Fiber	Default value is 04h	1
8012~8015	Minimum and Wavelength per Active Fiber	The value corresponds to QSFP28 I2C register(Address A0h, byte 186~189(Page 00))	1,2
8016~8017	Maximum per Lane Optical Width	Default value is 00h	1
8018~8019	Device Technology	The value corresponds to QSFP28 I2C register(Address A0h, byte 147(Page 00))	1,2
801A	Signal Code	Default value is 40h	1
801B~801C	Maximum Total Optical Output Power per Connector and Maximum Optical Input Power per Network Lane	Default value is 00h: undefined	1
801D	Maximum Power Consumption	Default value is 00h: undefined	1
801E	Maximum Power Consumption in Low Power Mode	Default value is 64h: 2W	1
801F	Maximum Operating Case Temp Range	The value corresponds to QSFP28 I2C register(Address A0h, byte 190(Page 00))	1,2
8020	Minimum Operating Case Temp Range	Default value is 00h	1
8021~805B	Vendor information	Reserved for Vendor	1
805C~8067	Lot Code and CLEI Code	Default value is 00h	1
8068	CFP2 MSA Hardware Specification Revision Number	Default value is 0Ah: V1.0	1
8069	CFP MSA Management Interface Specification Revision Number	Default value is 18h: V2.4	1
806A~806B	Module Hardware Version Number	Default V1.0	1
806C~806D	Module Firmware Version Number	Default V1.0	1
806E	Digital Diagnostic Monitoring Type	Default value is 0Ch: power measurement type(average Power)	1
806F	Digital Diagnostic Monitoring Capability 1	Default value is 03h	1
8070	Digital Diagnostic Monitoring Capability 2	Default value is 0Eh	1
8071	Module Enhanced Options	Default value is 20h	1

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8072~8073	Maximum High-Power-up and TX-Turn-on Time	Default value is 01h	1
8074	Host Lane Signal Spec	Default value is 01h: CAUI	1
8075	Heat Sink Type	Default value is 00h	1
8076	Maximum TX-Turn-off Time	Default value is 0Ah	1
8077	Maximum High-Power-down Time	Default value is 01h	1
8078	Module Enhanced Options 2	Default value is 20h	1
8079~807A	Transmitter and Receiver Monitor Clock Options	Default value is 00h: not supported	1
807B~807C	Module Firmware B Version Number	Default value is 00h	1
807D	Maximum MDIO Ready Time	Default value is 03h	1
807E	CFP Extended Identifier	Default value is C0h	1
807F	CFP NVR 1 Checksum	The 8-bit unsigned sum of all CFP NVR 1 contents from address 8000h through 807Eh inclusive.	

CFP NVR 2 Table: Alarm/Warning Threshold Registers

HexAddr	Register Name	Description	Note
8080~8087	Transceiver Temp Alarm/Warning Threshold	The value corresponds to QSFP28 I2C Temp register(Address A0h, byte 128~135(Page 03))	1,2
8088~808F	VCC Alarm/Warning Threshold	The value corresponds to QSFP28 I2C VCC threshold register(Address A0h, byte 144~151(Page 03))	1,2
8090~80A7	Alarm/Warning Threshold	Reserved or undefined	1
80A8~80AF	Laser Bias Current Alarm/Warning Threshold	The value corresponds to QSFP28 I2C Tx Bias threshold register(Address A0h, byte 184~191(Page 03))	1,2
80B0~80B7	Laser Output Power Alarm/Warning Threshold	The value corresponds to QSFP28 I2C TX Power threshold register(Address A0h, byte 192~199(Page 03))	1,2
80C0~80C7	Receive Optical Power Alarm/Warning Threshold	The value corresponds to QSFP28 I2C RX Power threshold register(Address A0h, byte 176~183(Page 03))	1,2
80C8~80FE	Alarm/Warning Threshold	Reserved or undefined	1
80FF	CFP NVR 2 Checksum	The 8-bit unsigned sum of all CFP NVR 2 contents from address 8080h through 80FEh inclusive.	

CFP Module VR 1. CFP Module level control and DDM registers.

HexAddr	Register Name	Description	Note
A01F	Module Alarms and Warnings 1	The value corresponds to QSFP28 I2C Alarms and Warning register(Address A0h, byte 6~7)	3
A02F	Module Temp Monitor A/D Value	The value corresponds to QSFP28 I2C Temp Monitor register(Address A0h, byte 22~23)	3
A030	Module Power supply 3.3 V Monitor A/D Value	The value corresponds to QSFP28 I2C Supply Voltage register(Address A0h, byte 26~27)	3

Network Lane VR : Network Lane Specific Register and A/D value Measurement Registers

HexAddr	Register Name	Description	Note
A200~A203	Network Lane n Alarm and Warning	The value corresponds to QSFP28 I2C Channel Monitor Interrupt Flags register(Address A0h, byte 9~14)	3

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A210~A213	Network Lane n Fault and Status	The bit[4] and bit[7] values correspond to QSFP28 I2C Channel Status Interrupt Flags register(Address A0h, byte 3)	3
A2A0~A2A3	Network Lane n Laser Bias Current monitor A/D value	The value corresponds to QSFP28 Tx Bias monitor register(Address A0h, byte 42~49)	3
A2B0~A2B3	Network Lane n Laser Output Power monitor A/D value	The value corresponds to QSFP28 TxPower monitor register(Address A0h, byte 50~57)	3
A2D0~A2D3	Network Lane n Receiver Input Power monitor A/D value	The value corresponds to QSFP28 I2C RxPower monitor register(Address A0h, byte 34~41)	3

Note:

1. CFP NVR 1 and CFP NVR 2 Tables have initial values. If customer need access to CFP NVR 1and CFP NVR 2 Table, we can OPEN write access.
2. When QSFP28 module present, firstly, read values from QSFP28 I2C registers and maps into the CFP MDIO registers.
3. When QSFP28 module present, the alarm/warning data and DDM data update periodically during the whole operation of the module, the maximum data refresh period is 200ms.

CFP2 Connector Pin Descriptions

Part A: Bottom Row Pin Function Definition

Pin	Symbol	Type	I/O	Description
1	GND			
2	(TX_MCLKn)	CML	O	CML For optical waveform testing. Not used.
3	(TX_MCLKp)	CML	O	CML For optical waveform testing. Not used.
4	GND			
5	NC			
6	NC			
7	GND			3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
8	3.3V_GND			
9	3.3V			3.3V Module power Supply
10	3.3V			
11	3.3V			
12	3.3V			
13	3.3V_GND			
14	3.3V_GND			
15	VND_IO_A		I/O	Module vendor I/O A.
16	VND_IO_B		I/O	Module vendor I/O B.
17	PRG_CNTL1	LVC MOS w/PU	I	Programmable Control 1 set via MDIO, MSA default: TRXIC_RSTn – TX & RX IC reset. “0” = reset, “1” or NC = enabled or not used
18	PRG_CNTL2	LVC MOS w/PU	I	Programmable Control 2 set via MDIO, MSA default: Hardware Interlock LSB, “00” ≤3W, “01” ≤6W, “10” ≤9W, “11” or NC ≤12W= not used
19	PRG_CNTL3	LVC MOS w/PU	I	Programmable Control 3 set via MDIO, MSA default: Hardware Interlock MSB, “00” ≤3W, “01” ≤6W, “10” ≤9W, “11” or NC ≤12W= not used
20	PRG_ALARM1	LVC MOS	O	Programmable Alarm 1 set via MDIO, MSA default:HIPWR_ON, “1” = Module high power up completed, “0” = Module not high powered up

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21	PRG_ALARM2	LVC MOS	O	Programmable Alarm 2 set via MDIO,MSA default: MOD_READY,“1” = ready, “0” = not ready
22	PRG_ALARM3	LVC MOS	O	Programmable Alarm 3 set via MDIO, MSA default: MOD_FAULT, module fault detected, “1” = fault, “0” = no fault
23	GND	GND		
24	TX_DIS	LVC MOS w/PU	I	Transmitter Disable for all channels, “1” or NC = transmitter disabled, “0” = transmitter enabled
25	RX_LOS	LVC MOS	O	Receiver loss of optical signal on any channel, “1” = loss of signal, “0” = normal condition
26	MOD_LOPWR	LVC MOS w/PU	I	Module low power mode. “1” or NC = module in low power (safe) mode, “0” = power-on enabled
27	MOD_ABS	GND	O	Module Absent. “1” or NC = Module absent, “0” = module present. Pull-up resistor on Host
28	MOD_RSTn	LVC MOS w/PD	I	Module Reset. “0” = reset the module, “1” or NC = module enabled, Pull Down resistor in module
29	GLB_ALRMn	LVC MOS	O	Global Alarm. “0” = alarm condition in any MDIO alarm register, “1” = no alarm .Pull-up resistor on Host
30	GND			
31	MDC	1.2V CMOS	I	Management data clock (electrical specs as per IEEE std802.3-2012)
32	MDIO	1.2V CMOS	I/O	Management Data I/O bi-directional data (electrical specs as IEEE std802.3-2012)
33	PRTADR0	1.2V CMOS	I	MDIO port address bit 0
34	PRTADR1	1.2V CMOS	I	MDIO port address bit 1
35	PRTADR2	1.2V CMOS	I	MDIO port address bit 2
36	VND_IO_C		I/O	Module vendor I/O C.
37	VND_IO_D		I/O	Module vendor I/O D.
38	VND_IO_E		I/O	Module vendor I/O E.
39	3.3V_GND			
40	3.3V_GND			
41	3.3V			3.3V Module power Supply
42	3.3V			
43	3.3V			
44	3.3V			
45	3.3V_GND			
46	GND			
47	NC	CML	O	Received data output
48	NC	CML	O	Received data output
49	GND			
50	(RX_MCLKn)	CML	O	CML For optical waveform testing. Not used.
51	(RX_MCLKP)	CML	O	CML For optical waveform testing. Not used.
52	GND			

Part B: Top Row Pin Function Definition

Pin	Symbol	Description	Pin	Symbol	Description
104	GND		78	(REFCLKp)	Not used.
103	NC		77	GND	
102	NC		76	NC	
101	GND		75	NC	
100	TX3n	CML, Inverted Input Data	74	GND	
99	TX3p	CML, Input Data	73	RX3n	CML, Inverted Output Data
98	GND		72	RX3p	CML, Output Data
97	TX2n	CML, Inverted Input Data	71	GND	
96	TX2p	CML, Input Data	70	RX2n	CML, Inverted Output Data
95	GND		69	RX2p	CML, Output Data
94	NC		68	GND	
93	NC		67	NC	
92	GND		66	NC	
91	NC		65	GND	
90	NC		64	NC	
89	GND		63	NC	
88	TX1n	CML, Inverted Input Data	62	GND	
87	TX1p	CML, Input Data	61	RX1n	CML, Inverted Output Data
86	GND		60	RX1p	CML, Output Data
85	TX0n	CML, Inverted Input Data	59	GND	
84	TX0p	CML, Input Data	58	RX0n	CML, Inverted Output Data
83	GND		57	RX0p	CML, Output Data
82	NC		56	GND	
81	NC		55	NC	
80	GND		54	NC	
79	(REFCLKn)	Not used.	53	GND	

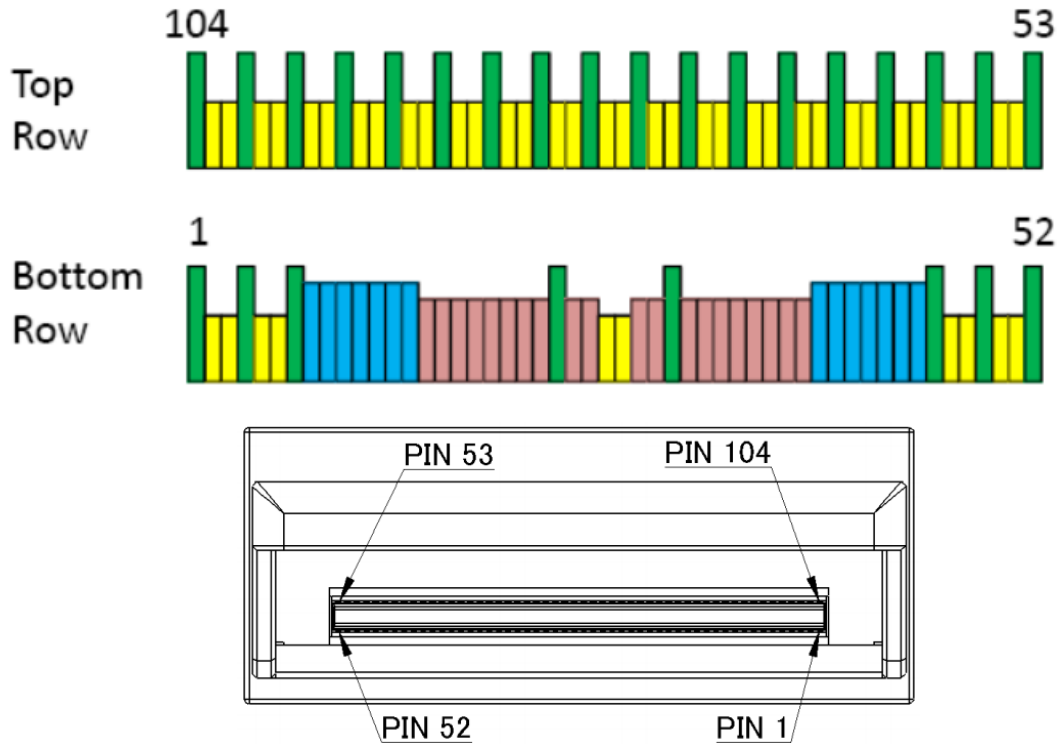


Figure2. Pad Layout of the CFP2 connector

QSFP28 Connector Pin Descriptions

Pin	Logic	Symbol	Description	Notes
1		GND	Module Ground	1
2	CML-O	Tx2-	Transmitter inverted data output	
3	CML-O	Tx2+	Transmitter non-inverted data output	
4		GND	Module Ground	1
5	CML-O	Tx4-	Transmitter inverted data output	
6	CML-O	Tx4+	Transmitter non-inverted data output	
7		GND	Module Ground	1
8	LVTTL-O	MODSEIL	Module Select	2
9	LVTTL-O	ResetL	Module Reset	2
10		VCCR _x	+3.3v Receiver Power Supply	
11	LVC MOS-O	SCL	2-wire Serial interface clock	2
12	LVC MOS-I/O	SDA	2-wire Serial interface data	2
13		GND	Module Ground	1
14	CML-I	RX3+	Receiver non-inverted data input	
15	CML-I	RX3-	Receiver inverted data input	
16		GND	Module Ground	1

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17	CML-I	RX1+	Receiver non-inverted data input	
18	CML-I	RX1-	Receiver inverted data input	
19		GND	Module Ground	1
20		GND	Module Ground	1
21	CML-I	RX2-	Receiver inverted data input	
22	CML-I	RX2+	Receiver non-inverted data input	
23		GND	Module Ground	1
24	CML-I	RX4-	Receiver inverted data input	
25	CML-I	RX4+	Receiver non-inverted data input	
26		GND	Module Ground	1
27	LVTTL-I	ModPrsL	Module Present, QSFP28 Module pulled down to GND	
28	LVTTL-I	IntL	Interrupt input	2
29		VCCTx	+3.3v Transmitter Power Supply	
30		VCC1	+3.3v Power Supply	
31	LVTTL-O	LPMode	Low Power Mode	2
32		GND	Module Ground	1
33	CML-O	Tx3+	Transmitter non-inverted data output	
34	CML-O	Tx3-	Transmitter inverted data output	
35		GND	Module Ground	1
36	CML-O	Tx1+	Transmitter non-inverted data output	
37	CML-O	Tx1-	Transmitter inverted data output	
38		GND	Module Ground	1

Notes:

1. Module circuit ground is isolated from module chassis ground within the module.
2. Open collector; pulled up with 4.7k ohms on the adapter board to a voltage 3.3V.

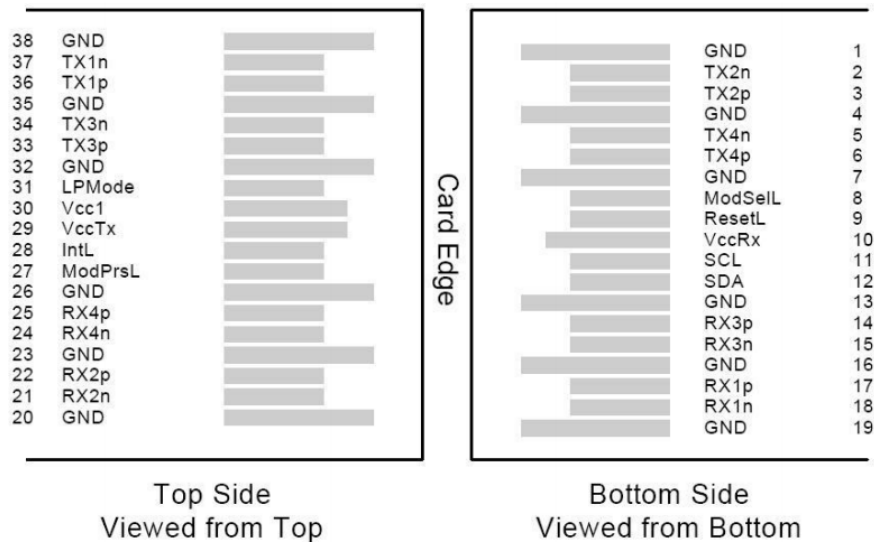


Figure3. Pad Layout of the QSFP28connector

Mechanical Dimensions

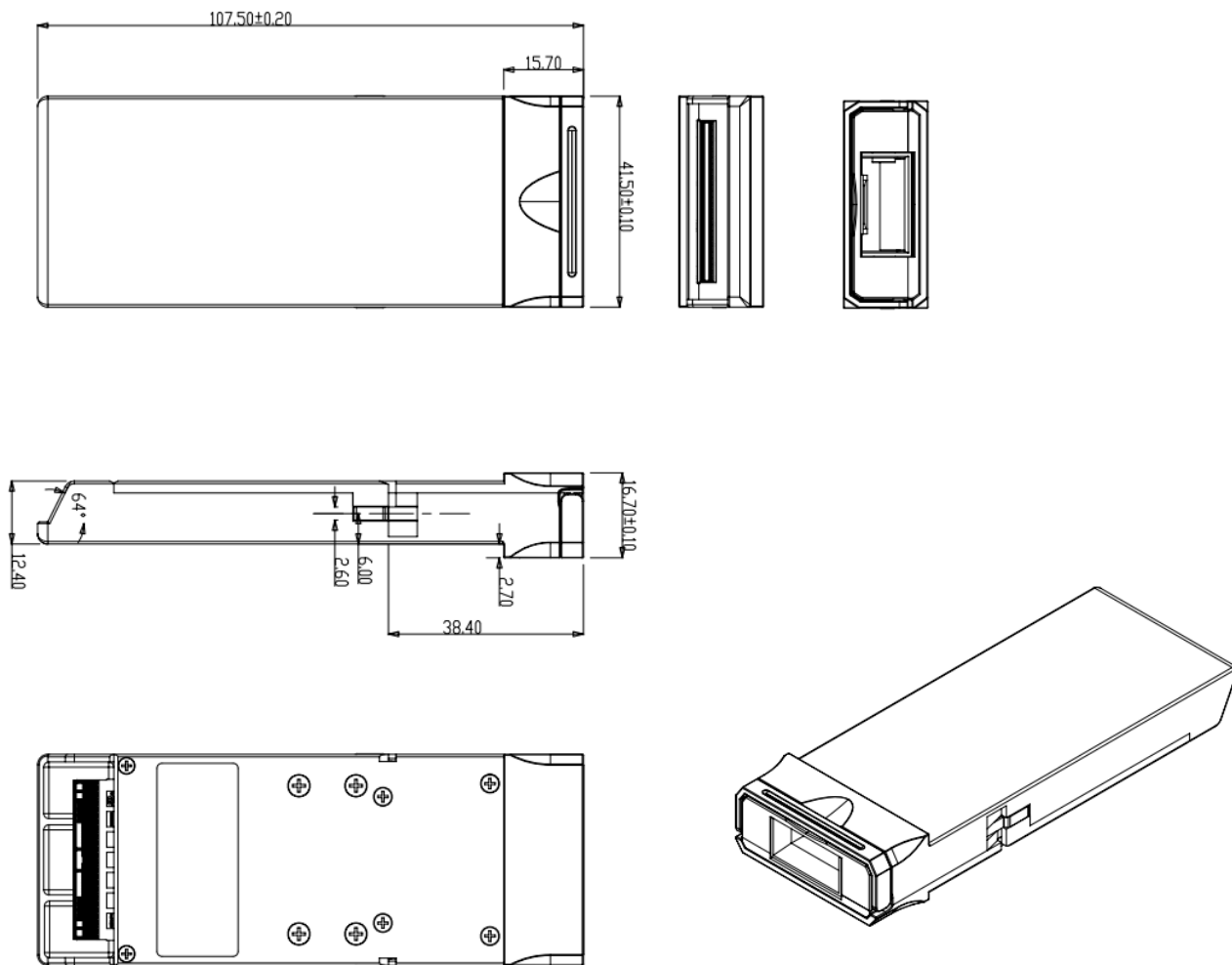


Figure4. Mechanical Specifications

Shenzhen Sourcelight Technology Co., Ltd

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