

CFP2 100G 40KM SMF

SLCF2-100G-ER4



Overview

Sourcelight's SLCF2-100G-ER4 are designed for use in 100 Gigabit Ethernet and 4x28G OTN client interfaces over single mode fiber.

They are compliant with the CFP MSA1, IEEE 802.3ba and OTU4 4I1-9D1F requirements specified in ITU-T Recommendations G.959.1/G.709 and Supplement 39 (G.sup39). Digital diagnostics functions are available via the MDIO interface, as specified by the CFP MSA. The transceiver is RoHS-6 compliant and lead-free per Directive 2002/95/EC3.

Features

- ◆ Direct LC receptacle optical interface
- ◆ Single +3.3V power supply
- ◆ Hot-pluggable
- ◆ Operating optical data rate up to 112Gbps
- ◆ Transmission distance up to 40km
- ◆ AC coupling of CML signals
- ◆ 1310 nm window cooled EA-DFB LD
- ◆ Integrated SOA, PIN ROSA and TOSA
- ◆ Low power dissipation(Max:9W)
- ◆ Built in digital diagnostic function
- ◆ Operating case temperature range: 0°C to 70°C
- ◆ Compliant with RoHs
- ◆ MDIO Communication Interface

Applications

- ◆ Local and wide area network (LAN and WAN)
- ◆ Ethernet switches and router applications
- ◆ ITU-T OTU4 OTL4.4 applications

Ordering Information

Part Number	Product Description
SLCF2-100G-ER4	CFP2 100G 1310nm ER4 40Km SMF LC

General Specifications

Parameter	Symbol	Min	Typical	Max	Units	Note
Bit Rate (all wavelengths combined)	BR	103.1		112.0	Gb/s	
Bit Error Ratio @25.78Gb/s	BER1			10 ⁻¹²		
Bit Error Ratio @27.95Gb/s	BER2			10 ⁻⁶		
Maximum Supported Distances	Lmax1			40	Km	

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Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	Vcc	-0.5	+3.6	V
Storage Temperature	Tst	-40	85	°C
Case Operating Temperature	Top	-5	75	°C
Relative Humidity	Rh	5	85	%
Receiver Damage Threshold, per Lane	PRdmg	5.5		dBm

Supply Voltage Electrical Characteristics

Parameter	Symbol	Min	Typical	Max	Units	Note
Supply Current	Icc			2.75	A	1
Power Supply Noise	Vrip			2%		DC-1MHz
				3%		1-10MHz
Dissipation	Pw			9	W	Class3
Low Power Dissipation	Plow			2	W	
Inrush Current	I-inrush			200	mA/usec	Class3
Turn-off Current	I-turnoff	-200			mA/usec	Class3

Different Signal Electrical Characteristics

Parameter	Symbol	Min	Typical	Max	Units	Note
Single Ended Data Input Swing		55		525	mV	
Single Ended Data Output Swing		150		500	mV	
Differential Signal Output Resistance		80		120	Ω	
Differential Signal Input Resistance		80		120	Ω	

3.3V LVC MOS Electrical Characteristics

Parameter	Symbol	Min	Typical	Max	Units	Note
Input High Voltage	3.3VIH	2.0		Vcc+0.3	V	
Input Low Voltage	3.3VIL	-0.3		0.8	V	
Input Leakage Current	3.3IIN	-10		+10	uA	
Output High Voltage	3.3VOH	Vcc-0.2			V	(IOH=100uA)
Output Low Voltage	3.3VOL			0.2	V	(IOL=100uA)
Minimum Pulse Width of Control Pin Signal	t_CNTL	100			us	

1.2V LVC MOS Electrical Characteristics

Parameter	Symbol	Min	Typical	Max	Units	Note
Input High Voltage	1.2VIH	0.84		1.5	V	
Input Low Voltage	1.2VIL	-0.3		0.36	V	
Input Leakage Current	1.2IIN	-100		+100	uA	
Output High Voltage	1.2VOH	1.0		1.5	V	
Output Low Voltage	1.2VOL	-0.3		0.2	V	
Output High Current	1.2IOH			-4	mA	
Output Low Current	1.2IOL	+4			mA	
Input Capacitance	Ci			10	pF	

Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Units	Note
Transmitter						
Signaling Rate for Each Lane (100GbE)			25.78125		Gb/s	
Signaling Rate for Each Lane (OTU4)			27.95249		Gb/s	
Four Lane Wavelength Range	λ_1	1294.53	1295.56	1296.59	Nm	
	λ_2	1299.02	1300.05	1301.09	Nm	
	λ_3	1303.54	1304.58	1305.63	Nm	
	λ_4	1308.09	1309.14	1310.19	nm	
Side Mode Suppression Ratio	SMSR	30			dB	
Total Average Launch Power	Pt			+8.9	dBm	
Average Launch Power for Each Lane	Pa	-2.5		+2.9	dBm	1
Optical Modulation Amplitude for Each Lane	OMA	-1.3		4.5	dBm	2
Transmitter and Dispersion Penalty for Each Lanes				1.5	TDP	
Average Launch Power of Off Transmitter for Each Lanes	Poff			-30	dBm	
Extinction Ratio	ER	8			dB	
RIN ₂₀ OMA				-130	dB/Hz	
Optical Return Loss Tolerance				20	dB	
Transmitter Reflectance				-12	dB	3
Eye Diagram		Compliant with IEEE 802.3ba-LR4/OTU4				
Receiver						
Signaling Rate for Each Lane (100GbE)			25.78125		Gb/s	
Signaling Rate for Each Lane (OTU4)			27.95249		Gb/s	

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Four Lane Wavelength Range	λ_1	1294.53	1295.56	1296.59	Nm	
	λ_2	1299.02	1300.05	1301.09	Nm	
	λ_3	1303.54	1304.58	1305.63	Nm	
	λ_4	1308.09	1309.14	1310.19	nm	
Overload Input Optical Power	Pmax	5.5			dBm	5
Average Receive Power per Lane (100GE)	RXPx	-20.9		4.5	dBm	5&6
Average Receive Power per Lane (OTU4)	RXPx	-23.2		4.5	dBm	
Receive Power (OMA) per Lane	RxOMA			4.5	dBm	
Difference in Receive Power between Any Two Lanes				4.5	dBm	
Receiver Sensitivity in OMA per Lane (100GbE) at BER= 1×10^{-12}	Rxsens			-21.4	dBm	7
Equivalent receiver sensitivity (OTU4)	S _{AVG}			-23.2	dBm	8
Stressed Receiver Sensitivity in OMA for Each Lane (100GbE)				-17.9	dBm	9&10
Los Assert	LOSA	-30			dBm	
Los De-assert	LOSD			-20.9	dBm	
Los Hysteresis		0.5			dBm	

Note:

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A transmitter with launch power below this value cannot be compliant; however, a value above this does not ensure compliance
2. Even if the TDP<1dB, the OMA (min) must exceed this value
3. Transmitter reflectance is defined looking into the transmitter
4. The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level
5. Minimum average receive power and maximum receiver sensitivity (OMA), each lane, is informative for 100GBase-LR4
6. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance
7. Receiver sensitivity (OMA), each lane (max) is informative
8. Measured with PRBS 2³¹-1 for BER= 10^{-5} . The BER for the OTU4 application is required to be met only after FEC has been applied.
9. Measured with conformance test signal at TP3 for BER= 10^{-12}
10. Conditions of stressed receiver sensitivity test: vertical eye closure penalty for each lane is 1.8dB; stressed eye J2 Jitter for each lane is 0.3UI; stressed eye J9 Jitter for each lane is 0.47UI.

Recommended Operating Environment

Parameter	Symbol	Min.	Typical	Max	Unit
Power Supply Voltage	V _{CC}	3.2	3.3	3.4	V
Operating Case Temperature	T _C	0		70	°C
Data rate			103.125	112	Gb/s

Pin Descriptions

	Top Row		Bottom Row		Top Row		Bottom Row
104	GND	1	GND	78	{REFCLKp}	27	MOD_ABS
103	N.C.	2	{TX_MCLKn}	77	GND	28	MOD_RSTn
102	N.C.	3	{TX_MCLKp}	76	N.C.	29	GLB_ALRMn
101	GND	4	GND	75	N.C.	30	GND
100	TX3n	5	N.C.	74	GND	31	MDC
99	TX3p	6	N.C.	73	RX3n	32	MDIO
98	GND	7	3.3V_GND	72	RX3p	33	PRTADR0
97	TX2n	8	3.3V_GND	71	GND	34	PRTADR1
96	TX2p	9	3.3V	70	RX2n	35	PRTADR2
95	GND	10	3.3V	69	RX2p	36	VND_IO_C
94	N.C.	11	3.3V	68	GND	37	VND_IO_D
93	N.C.	12	3.3V	67	N.C.	38	VND_IO_E
92	GND	13	3.3V_GND	66	N.C.	39	3.3V_GND
91	N.C.	14	3.3V_GND	65	GND	40	3.3V_GND
90	N.C.	15	VND_IO_A	64	N.C.	41	3.3V
89	GND	16	VND_IO_B	63	N.C.	42	3.3V
88	TX1n	17	PRG_CNTL1	62	GND	43	3.3V
87	TX1p	18	PRG_CNTL2	61	RX1n	44	3.3V
86	GND	19	PRG_CNTL3	60	RX1p	45	3.3V_GND
85	TX0n	20	PRG_ALRM1	59	GND	46	GND
84	TX0p	21	PRG_ALRM2	58	RX0n	47	N.C.
83	GND	22	PRG_ALRM3	57	RX0p	48	N.C.
82	N.C.	23	GND	56	GND	49	GND
81	N.C.	24	TX_DIS	55	N.C.	50	{RX_MCLKn}
80	GND	25	RX_LOS	54	N.C.	51	{RX_MCLKp}
79	{REFCLKn}	26	MOD_LOPWR	53	GND	52	GND

Figure1. Pin Descriptions

Bottom Row Pin Function Definition

The CFP2 connector has 104 pins which are arranged in Top and Bottom rows. The pin map is shown in Table below. The detailed description of the Bottom row ranges from pin 1 through pin 52 and is shown below. The pin orientation is shown below:

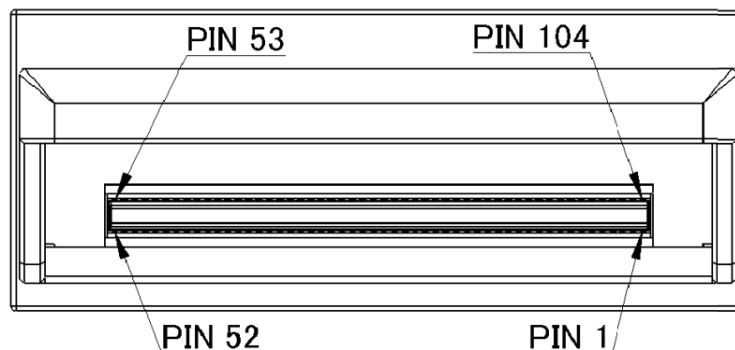


Figure2. CFP2 Pin Map Orientation

Bottom Row Pin Function Definition

PIN	Name	I/O	Logic	Description
1	GND			
2	TX_MCLKn			Supported.
3	TX_MCLKp			Supported.
4	GND			
5	N.C.			
6	N.C.			
7	3.3V_GND			3.3V Module Supply Voltage Return Ground, internally connected to Signal Ground
8	3.3V_GND			3.3V Module Supply Voltage Return Ground, internally connected to Signal Ground
9	3.3V			3.3V Module Supply Voltage
10	3.3V			3.3V Module Supply Voltage
11	3.3V			3.3V Module Supply Voltage
12	3.3V			3.3V Module Supply Voltage
13	3.3V_GND			3.3V Module Supply Voltage Return Ground, internally connected to Signal Ground
14	3.3V_GND			3.3V Module Supply Voltage Return Ground, internally connected to Signal Ground
15	VND_IO_A	I/O		Module Vendor I/O A. Do Not Connect!
16	VND_IO_B	I/O		Module Vendor I/O B. Do Not Connect!
17	PRG_CNTL1	I	LVC MOS w/ PUR	Programmable Control 1 set over MDIO
18	PRG_CNTL2	I	LVC MOS w/ PUR	Programmable Control 2 set over MDIO
19	PRG_CNTL3	I	LVC MOS w/ PUR	Programmable Control 3 set over MDIO
20	PRG_ALARM1	O	LVC MOS	Programmable Alarm 1 set over MDIO
21	PRG_ALARM2	O	LVC MOS	Programmable Alarm 2 set over MDIO
22	PRG_ALARM3	O	LVC MOS	Programmable Alarm 3 set over MDIO
23	GND			
24	TX_DIS	I	LVC MOS w/ PUR	Transmitter Disable for all lanes, "1" or NC = transmitter disabled, "0" = transmitter enabled
25	RX_LOS	O	LVC MOS	Receiver Loss of Optical Signal, "1": low optical signal, "0": normal condition
26	MOD_LOPW R	I	LVC MOS w/ PUR	Module Low Power Mode. "1" or NC: module in low power (safe) mode, "0": power-on enabled
27	MOD_ABS	O	GND	Module Absent. "1" or NC: module absent, "0": module present, Pull Up Resistor on Host
28	MOD_RSTn	I	LVC MOS w/ PDR	Module Reset. "0" resets the module, "1" or NC = module enabled, Pull Down Resistor in Module
29	GLB_ALRMn	O	LVC MOS	Global Alarm. "0": alarm condition in any MDIO Alarm register, "1": no alarm condition, Open Drain, Pull Up Resistor on Host
30	GND			
31	MDC	I/O	1.2V CMOS	Management Data I/O bi-directional data (electrical specs as per 802.3ae and ba)
32	MDIO	I	1.2V CMOS	Management Data Clock (electrical specs as per 802.3ae and ba)
33	PRTADRO	I	1.2V CMOS	MDIO Physical Port address bit 0

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34	PRTADR1	I	1.2V CMOS	MDIO Physical Port address bit 1
35	PRTADR2	I	1.2V CMOS	MDIO Physical Port address bit 2
36	VND_IO_C	I/O		Module Vendor I/O C. Do Not Connect!
37	VND_IO_D	I/O		Module Vendor I/O D. Do Not Connect!
38	VND_IO_E	I/O		Module Vendor I/O E. Do Not Connect!
39	3.3V_GND			3.3V Module Supply Voltage Return Ground, internally connected to Signal Ground
40	3.3V_GND			3.3V Module Supply Voltage Return Ground, internally connected to Signal Ground
41	3.3V			3.3V Module Supply Voltage
42	3.3V			3.3V Module Supply Voltage
43	3.3V			3.3V Module Supply Voltage
44	3.3V			3.3V Module Supply Voltage
45	3.3V_GND			3.3V Module Supply Voltage Return Ground, internally connected to Signal Ground
46	GND			
47	N.C.			
48	N.C.			
49	GND			
50	RX_MCLKn			Supported.
51	RX_MCLKp			Supported.
52	GND			

Block Diagram

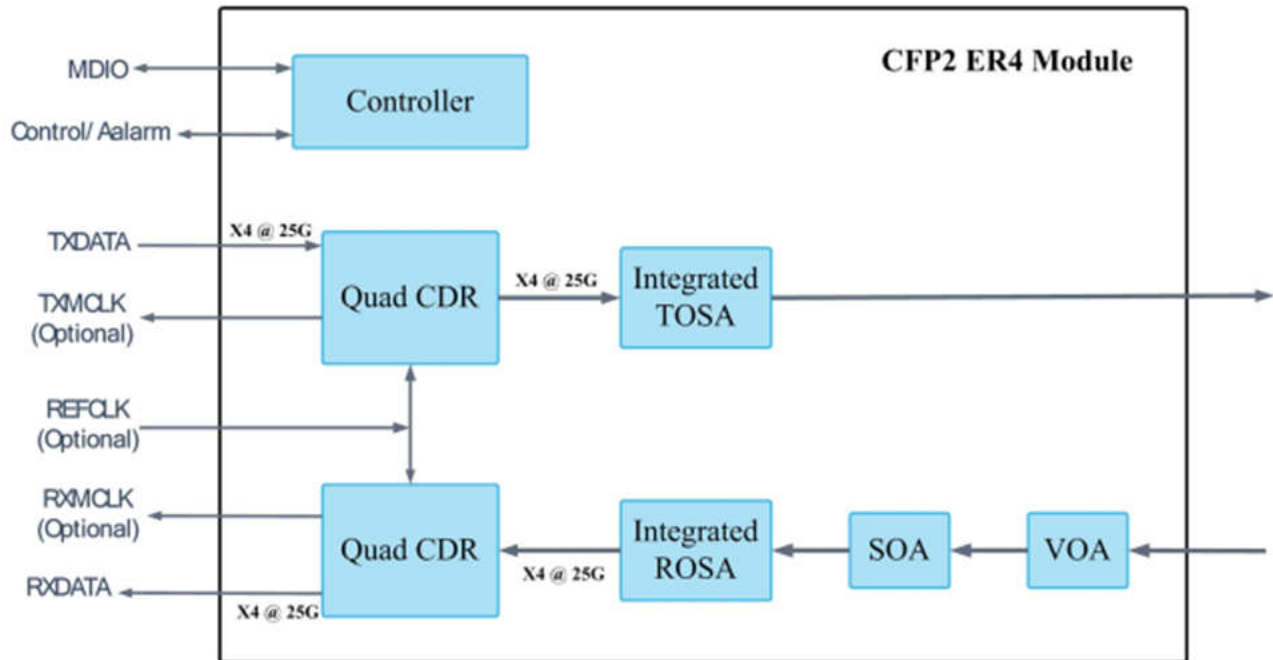


Figure3. CFP2 ER4 Block Diagram

Required Host Board Components

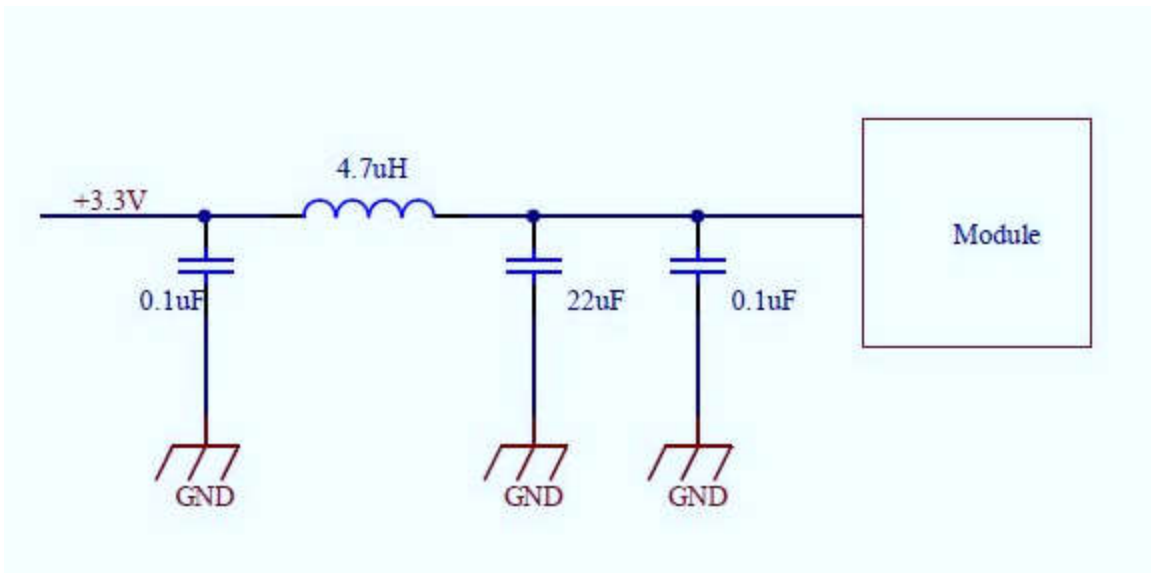


Figure4. CFP2 ER4 Required Host Board Components

Mechanical Dimensions

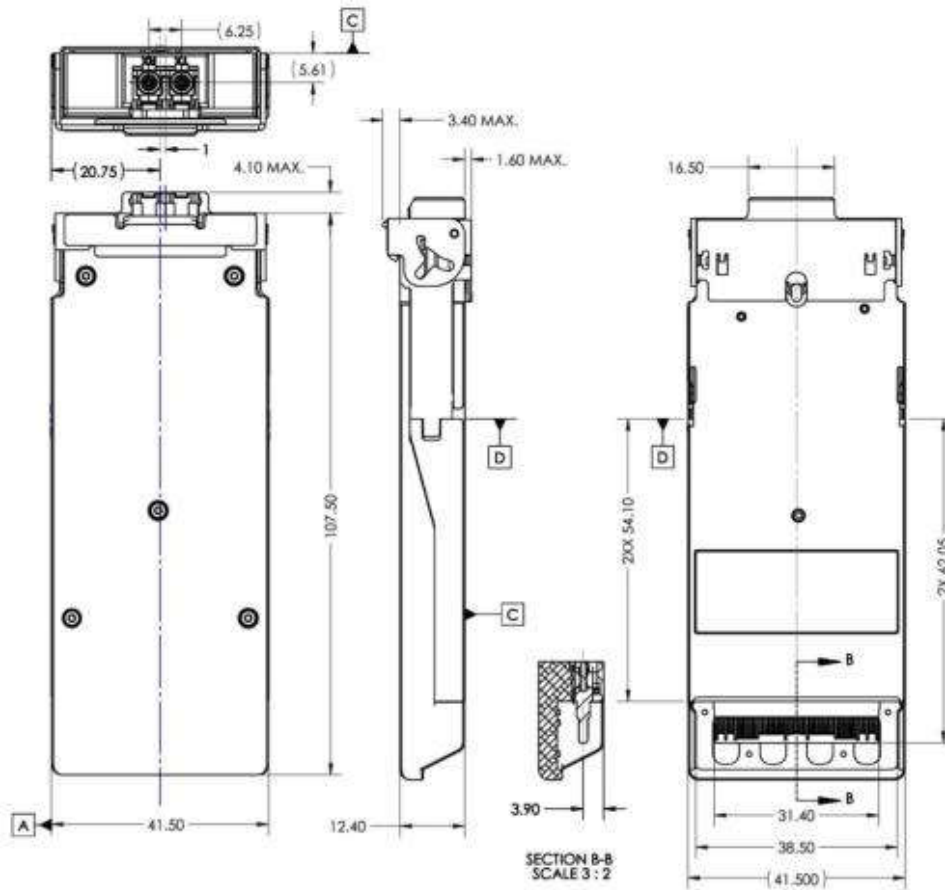


Figure5. Mechanical Specifications

Regulatory Compliance

Feature	Test Method	Performance
Electrostatic Discharge (ESD) to the Electrical Pins	MIL-STD-883E Method 3015.7	high speed signal pins shall withstand 500V electrostatic discharge based on Human Body Model per JEDEC JESD22-A114-B the other pins with exception of the high speed signal pins shall withstand 2kV electrostatic discharge based on Human Body Model per JEDEC JESD22-A114-B
Electrostatic Discharge (ESD) Immunity	IEC61000-4-2 Class B	15kV air discharges during operation and 8kV direct contact discharge
Electromagnetic Interference (EMI)	CISPR22 ITE Class B; FCC Class B; CENELEC; EN55022; VCCI Class 1	Compliant with standard
Immunity	IEC61000-4-3 Class 2	Compliant with any electro-magnetic regulations
Safety	FDA; CDRH 21-CFR 1040 Class 1; UL; TUV-GS; CE	

Shenzhen Sourcelight Technology Co., Ltd

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